

FIG. 1

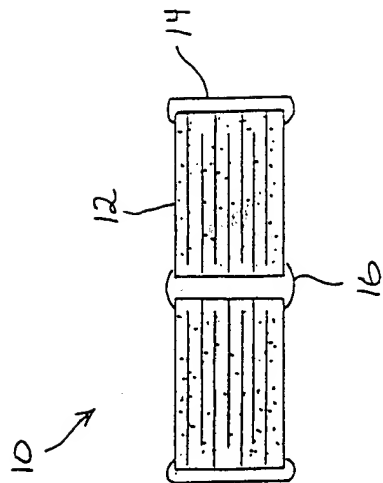


FIG. 2

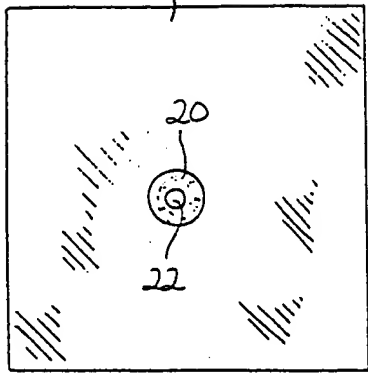


FIG. 3A

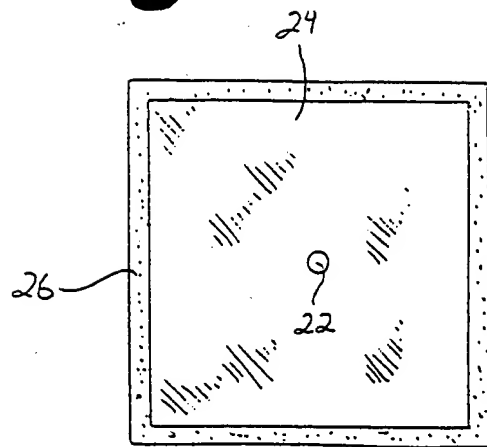


FIG. 3B

eg. VIA LAYOUT FOR CONTACTS FOR MICRO PROCESSOR

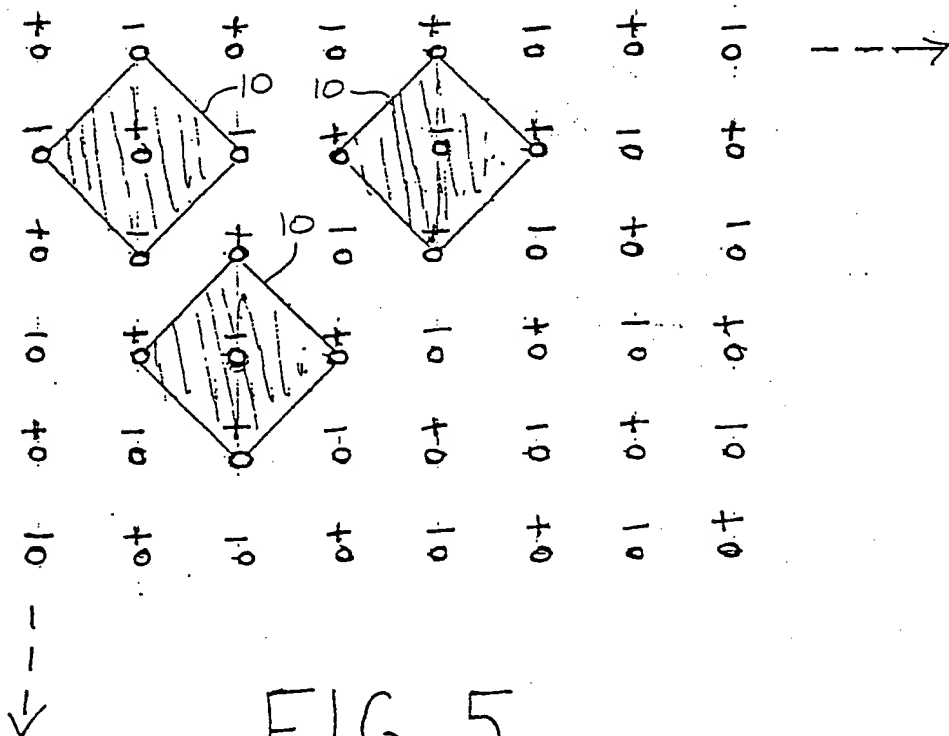


FIG. 5

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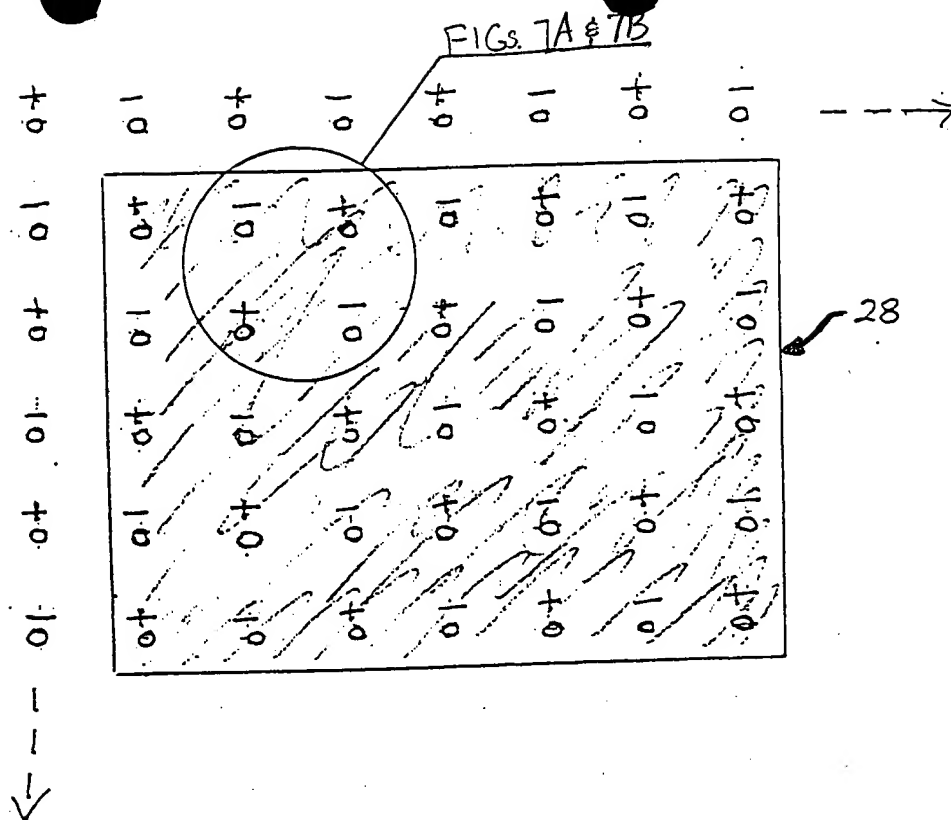


FIG. 6

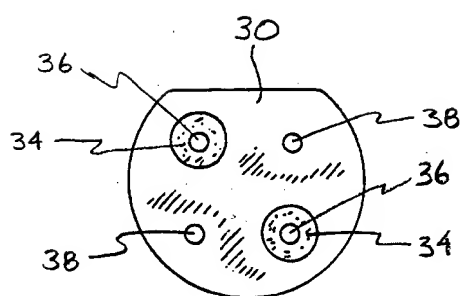


FIG. 7A

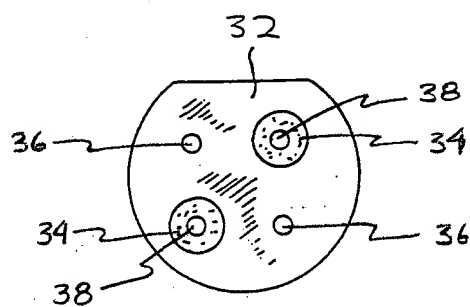


FIG. 7B